UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,698	03/05/2002	Brian N. Ripley	100202181-1	7441

7590 07/17/2009

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
ROJAS, MIDYS	
ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
07/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,698	RIPLEY, BRIAN N.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-20 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-20 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. As per Applicant's request, the examiner would like to clarify that the previous rejection, dated 3/7/07, was indeed a non-final rejection.

Response to Arguments

2. Applicant's arguments filed on 10/23/07 have been considered but are not persuasive.

Applicant argues that Lee et al. in view of Chan et al. does not teach a variable width mapping process provides a correlation between said single cell variable width memory locations and said variable width register. However, Chan et al. discloses a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). Therefore, the variable cell size circuit must include a variable width register for the storage of the number of bytes, and as thus, represents the correlation between the variable width memory location and the variable width register.

Applicant also argues that the references relied upon do not teach a single cell variable width location identified by a unique internal identifier. However, the memory locations of Lee in view of Chan have individual addresses (memory row address, memory column strobe, Page 2, paragraph 19) and therefore, are identified by unique internal identifiers. Such addresses are part of a mapping system used at the time of access, as implemented in the memory controller 410. The addresses represent unique identifiers.

Regarding Claims 4-5, Applicant argues that the references relied upon do not teach "single cell variable width memory locations identified by a unique internal identifier which is referenced by said controller to access aid each one of said plurality of single cell variable width

memory locations". The examiner disagrees. The memory locations of Lee in view of Chan have individual addresses (memory row address, memory column strobe, Page 2, paragraph 19) and therefore, are identified by unique internal identifiers. In making access requests, the addresses are used by the controller. Additionally, such addresses are part of a mapping system used at the time of access implemented in the memory controller 410.

Regarding Claim 7, Applicant argues that the references relied upon do not teach "the bit width of at least one of said plurality of single cell variable width memory locations is configured in accordance with criteria directed at decreasing processor operations". The examiner disagrees. Lee in view of Chan discloses variably configuring the width (page size) of the memory in order to achieve a reduction delay by increasing page hit rate (processor operations) thus decreasing power consumption (paragraph 0008).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14, 16-20, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (2003/0158995) in view of Chan et al. (6,230,249).

Regarding Claim 1, Lee discloses a variable width memory system comprising (DRAM control with adjustable page size):

a bus for communicating information (Figure 1, exemplary system, buses 160, 170);

a plurality of memory locations coupled to said bus (memory locations of memory 140), said plurality of variable width memory locations store information (DRAM access, Abstract, wherein storing is an accesses), wherein said plurality of variable width memory locations receive a number of bits corresponding to the width of the variable memory locations (determining adjustable page portion, Claim 1); and a controller coupled to said bus 410 (Figure 4), said controller directs access to said plurality of variable width memory locations being accessed (page 2, paragraphs 18 and 19). Being that the memory has variable widths (page size), the number of widths accessed depends of the current width of the memory location accessed. Additionally, since the page width is determined for each access, all memory pages do not have to have the same width.

Lee does not teach the variable width memory locations being single cell memory locations and receiving a number of bits in the single cell memory locations corresponding to the width of a variable width register. Chan et al. discloses a system with a FIFO memory device containing programmable variable cell sizes (see Abstract and Col. 2, line 65- Col. 3, line 14). The system of Chan teaches a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Lee to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the new variable memory cells since variable memory cells provides

for a more flexible memory device that may be suited for more applications (see Chan Col. 1, lines 47-55 for motivation).

The variable cell size circuit of Chan et al. includes a counter and a comparator both of which store values for their functions. Therefore, the variable cell size circuit must also include a register for the storing of these values (Col. 1, lines 59-66). Additionally, the variable cell size circuit controls successive accesses to a cell in the memory device (Abstract). Since this circuit is a control structure it must include a processing unit and therefore its register is in a processor associated (correlation) with the variable width memory system.

Regarding Claim 2, Lee in view of Chan discloses variable width memory locations 420 included on a single memory substrate (see Figure 4).

Regarding Claim 3, the memory of Lee can be implemented a DRAM (abstract).

Regarding Claims 4-5, the memory locations of Lee in view of Chan have individual addresses (memory row address, memory column strobe, Page 2, paragraph 19) and therefore, are identified by unique internal identifiers. In making access requests, the addresses are used by the controller. Additionally, such addresses are part of a mapping system used at the time of access implemented in the memory controller 410.

Regarding Claim 6, in the system of Lee in view of Chan, two memory locations could have the same width (page size) depending on the parameters being used and in what the page sizes are determined to be in step 520 (Figure 5, and paragraphs 0025-0026).

Regarding Claim 7, Lee in view of Chan discloses variably configuring the width (page size) of the memory in order to achieve a reduction delay by increasing page hit rate (processor operations) thus decreasing power consumption (paragraph 0008).

Regarding Claim 8 and 14, Lee et al. discloses a variable width memory (Fig. 1, 140) comprising receiving a register indicator corresponding to a register (internal address provided from the requester); accessing a memory cell (memory controller multiplexes row and column address to system memory) based on said register indicator, wherein said memory cell is allocated a storage size correlating to the bit capacity of said register (determine page size, Figure 5); and transferring information between said memory cell and another component (data is transferred between memory controller and system memory 420, paragraph 0019), wherein said information includes the same number of bits as said bit capacity, and varying the bit capacity on a per access basis to the memory cell automatically (Figure 5). Being that the memory has variable widths (page size), the number of widths accessed depends of the current width of the memory location accessed. Additionally, since the page width is determined for each access, all memory pages do not have to have the same width.

Lee does not teach the variable width memory locations being single cell memory locations and receiving a number of bits in the single cell memory locations corresponding to the width of a register. Chan et al. discloses a system with a FIFO memory device containing programmable variable cell sizes (see Abstract and Col. 2, line 65- Col. 3, line 14). The system of Chan teaches a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Lee to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the new variable memory cells since variable memory cells provides for a more flexible

memory device that may be suited for more applications (see Chan Col. 1, lines 47-55 for motivation).

The variable cell size circuit of Chan et al. includes a counter and a comparator both of which store values for their functions. Therefore, the variable cell size circuit must also include a register for the storing of these values (Col. 1, lines 59-66). Additionally, the variable cell size circuit controls successive accesses to a cell in the memory device (Abstract). Since this circuit is a control structure it must include a processing unit and therefore its register is in a processor associated (correlation) with the variable width memory system.

Regarding Claims 9, the register indicator (memory address) is received from a processor (requester). Page 2, paragraph 0018.

Regarding Claim 10, the bit capacity is determined (Figure 5) by processing criteria (input from requester) associated with a processor.

Regarding Claim 11, the data being transferred (see Figure 4) is in the form of a packet wherein packets are a group of bits or bytes of information.

Regarding Claim 12, the information being transferred to and from the memory also includes information such as column address strobe, row address strobe, and write enable (paragraph 0019). These commands are associated with certain fields in the memory and participate in the performance of accessing functions for completing such commands.

Regarding Claim 13, the information being transferred that is associated with certain fields (row and column address information) is sequentially received and taken in by the memory 420 (see Figure 4).

Regarding Claim 20, Lee et al. discloses a variable memory width assignment method (Figure 5) comprising analyzing a data block configuration specification (as part of determining process 520, Figure 5); identifying bits in a portion of said block of data while variably configuring the width (page size) of the memory in order to achieve a reduction delay by increasing page hit rate (processor operations) thus decreasing power consumption (paragraph 0008); and assigning a memory location width equal to said number of bits in said portion of said block of data (produce an adjustable page portion for prior access… Page 3, paragraph 0023), the data being transferred (see Figure 4) is in the form of a packet wherein packets are a group of bits or bytes of information; this information also includes column address strobe, row address strobe, and write enable (paragraph 0019). These commands are associated with certain fields in the memory and participate in the performance of accessing functions for completing such commands; they are sequentially received and taken in by the memory 420 (see Figure 4).

Being that the memory has variable widths (page size), the number of widths accessed depends of the current width of the memory location accessed. Additionally, since the page width is determined for each access, all memory pages do not have to have the same width.

Lee does not teach the variable width memory locations being single cell memory locations and receiving a number of bits in the single cell memory locations corresponding to the width of a variable width register. Chan et al. discloses a system with a FIFO memory device containing programmable variable cell sizes (see Abstract and Col. 2, line 65- Col. 3, line 14). The system of Chan teaches a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). It would have been obvious to one of ordinary skill in the art at the time

the invention was made to modify the system of Lee to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the new variable memory cells since variable memory cells provides for a more flexible memory device that may be suited for more applications (see Chan Col. 1, lines 47-55 for motivation).

The variable cell size circuit of Chan et al. includes a counter and a comparator both of which store values for their functions. Therefore, the variable cell size circuit must also include a register for the storing of these values (Col. 1, lines 59-66). Additionally, the variable cell size circuit controls successive accesses to a cell in the memory device (Abstract). Since this circuit is a control structure it must include a processing unit and therefore its register is in a processor associated (correlation) with the variable width memory system.

Regarding Claims 16-18, as in all memories, the variable page size memory of Lee et al. has many memory locations uniquely identified by memory addresses, which could be known as external identifiers (paragraph 0018) and these are used in accessing the adjustable memory pages (locations of various widths, paragraph 0010).

Regarding Claim 19, Lee et al. discloses an adjustable page size memory system, which arranges incoming bits in a contiguous manner during the write operation (paragraph 0019).

Regarding Claim 23, Lee et al. discloses a variable width memory (adjustable page size) assignment system (Abstract) comprising a means for communicating memory location identifiers (internal address provided by the requester); a means for storing information in a uniquely identifiable different width memory locations corresponding to said memory location identifiers (RAS# and CAS# are used to access adjustable pages within memory 420, Figure 4.

Paragraphs 0010 and 0018-0020), wherein said means for storing said information returns a number of bits equal to the width of one of said uniquely identifiable different width memory locations in response to a read request (read request, paragraph 0019); and a means for managing a connection with said uniquely identifiable different width memory locations (DRAM controller 410), wherein said means for managing said connection supervises writing and reading of information to and from said uniquely identifiable different width memory location. Being that the memory has variable widths (page size), the number of widths accessed depends of the current width of the memory location accessed. Additionally, since the page width is determined for each access, all memory pages do not have to have the same width.

Lee does not teach the variable width memory locations being single cell memory locations and receiving a number of bits in the single cell memory locations corresponding to the width of a variable width register. Chan et al. discloses a system with a FIFO memory device containing programmable variable cell sizes (see Abstract and Col. 2, line 65- Col. 3, line 14). The system of Chan teaches a variable cell size circuit 200 that defines the number of bytes (number of bits that will be received in a memory location) per cell for an access operation to a cell (Col. 5, lines 2-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Lee to include the variable width memory cells of Chan as well as the variable cell size circuit and further more, apply its variable memory location control method to the new variable memory cells since variable memory cells provides for a more flexible memory device that may be suited for more applications (see Chan Col. 1, lines 47-55 for motivation).

The variable cell size circuit of Chan et al. includes a counter and a comparator both of which store values for their functions. Therefore, the variable cell size circuit must also include a register for the storing of these values (Col. 1, lines 59-66). Additionally, the variable cell size circuit controls successive accesses to a cell in the memory device (Abstract). Since this circuit is a control structure it must include a processing unit and therefore its register is in a processor associated (correlation) with the variable width memory system.

Regarding Claim 24, Lee in view of Chan discloses the variable width memory assignment system wherein said means for managing said connection (memory controller 410) includes a means for tracking a correspondence between said uniquely identifiable variable memory widths and register identifiers (asserts RAS# and CAS# signals from internal address provided by requester, paragraphs 0018-0019).

Regarding Claim 25, Lee in view of Chan discloses the variable width memory assignment system wherein said register identifiers are provided by a means for processing said information (internal address provided by requester, paragraph 0018).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185

/Midys Rojas/
Midys Rojas
Examiner
Art Unit 2185

MR